

1 1. A multi-layered circuit structure, comprising:

2 a first substrate having conductive via through holes disposed therein; and

3 a second substrate laminated to said first substrate and having conductive,
4 adhesive-filled via through holes that align with, and make electrical
5 contact with, the conductive via through holes of said first substrate upon
6 lamination of said first and second substrates.

2. The multi-layered circuit structure in accordance with claim 1, wherein said
first substrate comprises a signal core layer, and said second substrate comprises a power
core layer.

3. The multi-layered circuit structure in accordance with claim 1, wherein said
first substrate comprises a pair of outer signal core layers, and said second substrate
comprises an inner power core layer sandwiched between said pair of outer signal core
layers.

1 4. The multi-layered circuit structure in accordance with claim 3, wherein said via
2 through holes of said inner power core layer comprise undercut contact surfaces, and said
3 via through holes of said signal layer have metallic pads that make electrical contact with
4 said undercut contact surfaces of said via through holes of said inner power core layer.

1 5. A multi-layered circuit structure, comprising:

2 a first substrate having conductive via through holes disposed therein; and

3 a second substrate laminated to said first substrate, and having via through
4 holes comprising conductive adhesive coated pads that align with, and
5 make electrical contact with, the conductive via through holes of said first
6 substrate upon lamination of said first and second substrates.

1 6. The multi-layered circuit structure in accordance with claim 5, wherein said
2 first substrate comprises a signal core layer, and said second substrate comprises a power
3 core layer.

1 7. The multi-layered circuit structure in accordance with claim 5, wherein said
2 first substrate comprises a pair of outer signal core layers, and said second substrate
3 comprises an inner power core layer sandwiched between said pair of outer signal core
4 layers.

1 8. A method of fabricating a multi-layered circuit, comprising the steps of:

2 filling via through holes of a first substrate with conductive adhesive;

3 aligning said via through holes of said first substrate with conductive via
4 through holes of a second substrate; and

5 laminating together said first and second substrates.

1 9. The method in accordance with claim 8, wherein said first substrate comprises
2 a signal core layer, and said second substrate comprises a power core layer.

1 10. The method in accordance with claim 8, wherein said first substrate
2 comprises a pair of outer signal core layers, and said second substrate comprises an inner
3 power core layer sandwiched between said pair of outer signal core layers.

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